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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,672	02/19/2004	Gordon D. McIntosh	AUS920031082US1	5246

35525 7590 07/12/2007
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EXAMINER	
HA, LEYNNA A	

ART UNIT	PAPER NUMBER
2135	

MAIL DATE	DELIVERY MODE
07/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/782,672	Applicant(s) MCINTOSH, GORDON D.	
	Examiner LEYNNA T. HA	Art Unit 2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 19 February 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 is pending.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 11-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 11 recites a computer program product in a computer readable medium where support can be found in the specification on pg. 28. Specification discloses:

> the processes of the present invention are capable of being distributed in the form of a computer readable medium of instructions and a variety of forms and that the present invention applies equally regardless of the particular type of signal bearing media actually used to carry out the distribution. Examples of computer readable media include recordable-type media, such as a floppy disk, a hard disk drive, a RAM, CD-ROMs, DVD-ROMs, and transmission-type media, such as digital and analog communications links, wired or wireless communications links using transmission forms, such as, for example, radio frequency and light wave transmissions.

Although, claim 11 is identified as a computer readable medium, the computer program product in a computer readable medium is directed to non-functional descriptive material that is capable of being distributed in the form of instructions and signals used to carry out distribution and transmission.

MPEP: **2106.01 [R-5]** **> Computer-Related Nonstatutory Subject Matter<

>Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and ***computer programs* which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works, and a compilation or mere arrangement of data.

When nonfunctional descriptive material is recorded on some computer-readable medium, in a computer or on ***an electromagnetic carrier signal***, it is not statutory since no requisite functionality is present to satisfy the practical application requirement. Merely claiming nonfunctional descriptive material, i.e., abstract ideas, stored on a computer-readable medium, in a computer, or ***on an electromagnetic carrier signal, does not make it statutory***. See Diehr, 450 U.S. at 185-86, 209 USPQ at 8 (noting that the claims for an algorithm in Benson were unpatentable as abstract ideas because "[t]he sole practical application of the algorithm was in connection with the programming of a general purpose computer."). Such a result would exalt form over substance. In re Sarkar, 588 F.2d 1330, 1333, 200 USPQ 132, 137 (CCPA 1978) ("[E]ach invention must be evaluated as claimed; yet semantogenic considerations preclude a determination based solely on words appearing in the claims. In the final analysis under § 101, the claimed invention, as a whole, must be evaluated for what it is.") (quoted with approval in Abele, 684 F.2d at 907, 214 USPQ at 687). See also In re Johnson, 589 F.2d 1070, 1077, 200 USPQ 199, 206 (CCPA 1978) ("form of the claim is often an exercise in drafting"). Thus, nonstatutory music is not a computer component, and it does not become statutory by merely recording it on a compact disk.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pickett, et al. (US 6,076,156), and further in view of Pechanek, et al. (US 6,848,041).

As per claim 1:

Pickett, et al. discusses a method in a data processing system for processing instructions by a processing unit, the method comprising:

[dynamically setting] an instruction set (col. 1, lines 35-36 and col.5, lines 21-32) for the processing unit using a selected instruction map (col.2, lines 33-40 and col.4, lines 31-36), wherein the selected instruction map is selected as one being different from a normal instruction map for the processing unit; and (col.9, lines 16-40 and col.11, lines 8-10)

processing the instructions at the processor using the instruction set (col.1, lines 22-64 and col.8, lines 41-60), wherein a set of authorized instructions are encoded using the selected instruction map. (col.9, lines 54-65 and col.12, lines 13-15)

Specification discloses the instruction map is also referred as an instruction decode map or an opcode map (pg.15). Specification further explains that encoded code is decoded by instruction decoder using an instruction set based on an instruction

map, such as opcode mapping is an opcode map that is identical to the opcode map selected from opcode map for use by remapping process to remap code into encoded code (pg.17). Thus, an instruction map can broadly be interpreted as instruction decode map, opcode map, mapped instructions/opcodes which is merely a mapping of a set of instructions.

Pickett discloses instructions are mapped to an opcode assigned to a redefinable instruction (e.g. a seldom used instruction selected during the design of the microprocessor to be redefinable to one or more of the added instructions) and allow for storage of the opcodes corresponding to the instructions selected for redefinition (col.2, lines 33-37 and col.4, lines 30-32). The application determine which instructions are remapped by setting the corresponding bit (col.4, lines 35-38 and col.8, lines 41-60). Thus, Pickett includes setting by assigning a set of instructions using a selected instruction map. However, Pickett did not include dynamically setting a set of instruction using a selected instruction map.

Pechanek, et al. discloses an invention that solves the problem of instruction set scability by defining a hierarchical instruction set (col.1, lines 44-50) where due to the variance in sequential and parallel code, a different set of instructions may be advantageously selected for a compact instruction set implementation in order to better optimize code density for each application (col.12, lines 5-9). Pechanek allow instructions to be dynamically constructed and plugged into the processor on a task by task basis (col.12, lines 15-18). Pechanek discloses specific bit encoding within Instruction Type (col.6, lines 8-10), simple fixed translations to a known state for a given

instruction mapping (col.10, lines 60-61 and col.13, lines 50-67), and the ability to independently select instructions within 3-bit address range in each function VIM (col.14, lines 30-38). Additionally, Pechanek discloses the use of an enhanced tool to support application analysis and the instruction selection process, is deemed advantageous (col.12, lines 26-29). Hence, the ability to dynamically create a set of compacted instructions on a task by task basis for the primary purpose of improving control and parallel code density (col.1, lines 57-61).

Therefore, it would have been obvious for a person of ordinary skills in the art to combine the teaching of Pickett with Pechanek teaching dynamically setting an instruction set using a selected instruction map because the ability to dynamically create a set of instructions on a task by task basis for the primary purpose of improving control and parallel code density (col.1, lines 57-61 and col.12, lines 6-29).

As per claim 2: See Pickett on col.4,lines 9-37 and Pechanek on col.1, lines 49-50; discussing the method of claim 1, wherein a new instruction map is selected each time the data processing system is started.

As per claim 3: See Pickett on col.1, lines 30-38; discussing the method of claim 1, wherein the instruction map is an opcode map.

As per claim 4: See Pickett on col.4,lines 29-42 and col.5, lines 21-37; discussing the method of claim 1 further comprising: encoding a set of instructions from a trusted computer base using the selected instruction map to form a set of encoded instructions; and sending the set of encoded instructions to the processing unit for execution.

As per claim 5: See Pickett on col.4,lines 40-41; discussing the method of claim 1, wherein the processing unit is at least one processor.

As per claim 6: See Pickett on col.6,lines 14-16; discussing the method of claim 4, wherein the encoding step and the sending step are performed by a program loader.

As per claim 7: See Pickett on col.1, lines 23-30; discussing the method of claim 1 further comprising: responsive to an event, executing a process to select the selected instruction map.

As per claim 8: See Pickett on col.2, lines 63-65 and Pechanek on col.15,lines 20-55; discussing the method of claim 7, wherein the process uses a machine serial number and a number of boot cycles to select the selected instruction map.

As per claim 9: See Pickett on col.1,lines 55-56; discussing the method of claim 7, wherein the event is at least one of an initialization of the data processing system and a user input.

As per claim 10: See Pickett on col.1,lines 50-64 and col.8,lines 33-40; discussing the method of claim 1, wherein the selected instruction set is set using a first selected instruction map when code is executed by a first privilege level and wherein a second selected instruction map is used as the instruction set for the processing unit when code is executed by a second privilege level.

As per claim 11:

Pickett, et al. discusses a computer program product in a computer readable medium for processing instructions by a processing unit in a data processing system, the computer program product comprising:

first instructions for *[dynamically setting]* an instruction set (col. 1, lines 35-36 and col.5, lines 21-32) for the processing unit using a selected instruction map (col.2, lines 33-40 and col.4, lines 31-36), wherein the selected instruction map is selected as one being different from a normal instruction map for the processing unit; and (col.9, lines 16-40 and col.11, lines 8-10)

second instructions for processing the instructions at the processor using the instruction set (col.1, lines 22-64 and col.8, lines 41-60), wherein a set of authorized instructions are encoded using the selected instruction map. (col., lines) (col.9, lines 54-65 and col.12, lines 13-15)

Specification discloses the instruction map is also referred as an instruction decode map or an opcode map (pg.15). Specification further explains that encoded code is decoded by instruction decoder using an instruction set based on an instruction map, such as opcode mapping is an opcode map that is identical to the opcode map selected from opcode map for use by remapping process to remap code into encoded code (pg.17). Thus, when applying art, specification is taken in light for variations to the instruction map terminology.

Pickett discloses instructions are mapped to an opcode assigned to a redefinable instruction (e.g. a seldom used instruction selected during the design of the microprocessor to be redefinable to one or more of the added instructions) and allow for storage of the opcodes corresponding to the instructions selected for redefinition (col.2, lines 33-37 and col.4, lines 30-32). The application determine which instructions are remapped by setting the corresponding bit (col.4, lines 35-38 and col.8, lines 41-60).

Thus, Pickett includes setting by assigning a set of instructions using a selected instruction map. However, Pickett did not include dynamically setting a set of instruction using a selected instruction map.

Pechanek, et al. discloses an invention that solves the problem of instruction set scability by defining a hierarchical instruction set (col.1, lines 44-50) where due to the variance in sequential and parallel code, a different set of instructions may be advantageously selected for a compact instruction set implementation in order to better optimize code density for each application (col.12, lines 5-9). Pechanek allow instructions to be dynamically constructed and plugged into the processor on a task by task basis (col.12, lines 15-18). Pechanek discloses specific bit encoding within Instruction Type (col.6, lines 8-10), simple fixed translations to a known state for a given instruction mapping (col.10, lines 60-61 and col.13, lines 50-67), and the ability to independently select instructions within 3-bit address range in each function VIM (col.14, lines 30-38). Additionally, Pechanek discloses the use of an enhanced tool to support application analysis and the instruction selection process, is deemed advantageous (col.12, lines 26-29). Hence, the ability to dynamically create a set of compacted instructions on a task by task basis for the primary purpose of improving control and parallel code density (col.1, lines 57-61).

Therefore, it would have been obvious for a person of ordinary skills in the art to combine the teaching of Pickett with Pechanek teaching dynamically setting an instruction set using a selected instruction map because the ability to dynamically create

a set of instructions on a task by task basis for the primary purpose of improving control and parallel code density (col.1, lines 57-61 and col.12, lines 6-29).

As per claim 12: See Pickett on col.4,lines 9-37 and Pechanek on col.1, lines 49-50; discussing the computer program product of claim 11, wherein a new instruction map is selected each time the data processing system is started.

As per claim 13: See Pickett on col.1, lines 30-38; discussing the computer program product of claim 11, wherein the instruction map is an opcode map.

As per claim 14: See Pickett on col.4,lines 29-42 and col.5, lines 21-37; discussing the computer program product of claim 11 further comprising: third instructions for encoding a set of instructions from a trusted computer base using the selected instruction map to form a set of encoded instructions; and fourth instructions for sending the set of encoded instructions to the processing unit for execution.

As per claim 15: See Pickett on col.4,lines 40-41; discussing the computer program product of claim 11, wherein the processing unit is at least one processor.

As per claim 16: See Pickett on col.6,lines 14-16; discussing the computer program product of claim 14, wherein the third instructions and the fourth instructions are performed by a program loader.

As per claim 17: See Pickett on col.1, lines 23-30; discussing the computer program product of claim 11 further comprising: third instructions, responsive to an event, for executing a process to select the selected instruction map.

As per claim 18: See Pickett on col.2, lines 63-65 and Pechanek on col.15,lines 20-55; discussing the computer program product of claim 17, wherein the process uses a

machine serial number and a number of boot cycles to select the selected instruction map.

As per claim 19: See Pickett on col.1,lines 55-56; discussing the computer program product of claim 17, wherein the event is at least one of an initialization of the data processing system and a user input.

As per claim 20: See Pickett on col.1,lines 50-64 and col.8,lines 33-40; discussing the computer program product of claim 11, wherein the selected instruction set is set using a first selected instruction map when code is executed by a first privilege level and wherein a second selected instruction map is used as the instruction set for the processing unit when code is executed by a second privilege level.

As per claim 21:

Pickett, et al. discusses a data processing system for processing instructions by a processing unit, the data processing system comprising:

[dynamically setting means for dynamically setting] an instruction set (col. 1, lines 35-36 and col.5, lines 21-32) for the processing unit using a selected instruction map (col.2, lines 33-40 and col.4, lines 31-36), wherein the selected instruction map is selected as one being different from a normal instruction map for the processing unit; and (col.9, lines 16-40 and col.11, lines 8-10)

processing means for processing the instructions at the processor using the instruction set (col.1, lines 22-64 and col.8, lines 41-60), wherein a set of authorized instructions are encoded using the selected instruction map. (col.9, lines 54-65 and col.12, lines 13-15)

Specification discloses the instruction map is also referred as an instruction decode map or an opcode map (pg.15). Specification further explains that encoded code is decoded by instruction decoder using an instruction set based on an instruction map, such as opcode mapping is an opcode map that is identical to the opcode map selected from opcode map for use by remapping process to remap code into encoded code (pg.17). Thus, when applying art, specification is taken in light for variations to the instruction map terminology.

Pickett discloses instructions are mapped to an opcode assigned to a redefinable instruction (e.g. a seldom used instruction selected during the design of the microprocessor to be redefinable to one or more of the added instructions) and allow for storage of the opcodes corresponding to the instructions selected for redefinition (col.2, lines 33-37 and col.4, lines 30-32). The application determine which instructions are remapped by setting the corresponding bit (col.4, lines 35-38 and col.8, lines 41-60). Thus, Pickett includes setting by assigning a set of instructions using a selected instruction map. However, Pickett did not include dynamically setting a set of instruction using a selected instruction map.

Pechanek, et al. discloses an invention that solves the problem of instruction set scability by defining a hierarchical instruction set (col.1, lines 44-50) where due to the variance in sequential and parallel code, a different set of instructions may be advantageously selected for a compact instruction set implementation in order to better optimize code density for each application (col.12, lines 5-9). Pechanek allow instructions to be dynamically constructed and plugged into the processor on a task by

task basis (col.12, lines 15-18). Pechanek discloses specific bit encoding within Instruction Type (col.6, lines 8-10), simple fixed translations to a known state for a given instruction mapping (col.10, lines 60-61 and col.13, lines 50-67), and the ability to independently select instructions within 3-bit address range in each function VIM (col.14, lines 30-38). Additionally, Pechanek discloses the use of an enhanced tool to support application analysis and the instruction selection process, is deemed advantageous (col.12, lines 26-29). Hence, the ability to dynamically create a set of compacted instructions on a task by task basis for the primary purpose of improving control and parallel code density (col.1, lines 57-61).

Therefore, it would have been obvious for a person of ordinary skills in the art to combine the teaching of Pickett with Pechanek teaching dynamically setting an instruction set using a selected instruction map because the ability to dynamically create a set of instructions on a task by task basis for the primary purpose of improving control and parallel code density (col.1, lines 57-61 and col.12, lines 6-29).

As per claim 22: See Pickett on col.4,lines 9-37 and Pechanek on col.1, lines 49-50; discussing the data processing system of claim 21, wherein a new instruction map is selected each time the data processing system is started.

As per claim 23: See Pickett on col.1, lines 30-38; discussing the data processing system of claim 21, wherein the instruction map is an opcode map.

As per claim 24: See Pickett on col.4,lines 29-42 and col.5, lines 21-37; discussing the data processing system of claim 21 further comprising: encoding means for encoding a set of instructions from a trusted computer base using the selected instruction map to

form a set of encoded instructions; and sending means for sending the set of encoded instructions to the processing unit for execution.

As per claim 25:

Pickett, et al. discusses a data processing system comprising:

a bus system; (col.12, lines 49-65)

a memory connected to the bus system, wherein the memory includes a set of instructions; and (col.12, lines 42-48)

a processing unit connected to the bus system (col.12, lines 40-42), wherein the processing unit executes a set of instructions to *[dynamically setting]* an instruction set (col. 1, lines 35-36 and col.5, lines 21-32) for the processing unit using a selected instruction map (col.2, lines 33-40 and col.4, lines 31-36), wherein the selected instruction map is selected as one being different from a normal instruction map for the processing unit; and (col.9, lines 16-40 and col.11, lines 8-10)

process the instructions at the processor using the instruction set (col.1, lines 22-64 and col.8, lines 41-60), wherein a set of authorized instructions are encoded using the selected instruction map. (col.9, lines 54-65 and col.12, lines 13-15)

Specification discloses the instruction map is also referred as an instruction decode map or an opcode map (pg.15). Specification further explains that encoded code is decoded by instruction decoder using an instruction set based on an instruction map, such as opcode mapping is an opcode map that is identical to the opcode map selected from opcode map for use by remapping process to remap code into encoded

code (pg.17). Thus, when applying art, specification is taken in light for variations to the instruction map terminology.

Pickett discloses instructions are mapped to an opcode assigned to a redefinable instruction (e.g. a seldom used instruction selected during the design of the microprocessor to be redefinable to one or more of the added instructions) and allow for storage of the opcodes corresponding to the instructions selected for redefinition (col.2, lines 33-37 and col.4, lines 30-32). The application determine which instructions are remapped by setting the corresponding bit (col.4, lines 35-38 and col.8, lines 41-60). Thus, Pickett includes setting by assigning a set of instructions using a selected instruction map. However, Pickett did not include dynamically setting a set of instruction using a selected instruction map.

Pechanek, et al. discloses an invention that solves the problem of instruction set scability by defining a hierarchical instruction set (col.1, lines 44-50) where due to the variance in sequential and parallel code, a different set of instructions may be advantageously selected for a compact instruction set implementation in order to better optimize code density for each application (col.12, lines 5-9). Pechanek allow instructions to be dynamically constructed and plugged into the processor on a task by task basis (col.12, lines 15-18). Pechanek discloses specific bit encoding within Instruction Type (col.6, lines 8-10), simple fixed translations to a known state for a given instruction mapping (col.10, lines 60-61 and col.13, lines 50-67), and the ability to independently select instructions within 3-bit address range in each function VIM (col.14, lines 30-38). Additionally, Pechanek discloses the use of an enhanced tool to

support application analysis and the instruction selection process, is deemed advantageous (col.12, lines 26-29). Hence, the ability to dynamically create a set of compacted instructions on a task by task basis for the primary purpose of improving control and parallel code density (col.1, lines 57-61).

Therefore, it would have been obvious for a person of ordinary skills in the art to combine the teaching of Pickett with Pechanek teaching dynamically setting an instruction set using a selected instruction map because the ability to dynamically create a set of instructions on a task by task basis for the primary purpose of improving control and parallel code density (col.1, lines 57-61 and col.12, lines 6-29).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEYNNA T. HA whose telephone number is (571) 272-3851. The examiner can normally be reached on Monday - Thursday (7:00 - 5:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on (571) 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LHa

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